AMENDMENTS TO THE SPECIFICATION:

Please replace the section entitled BRIEF DESCRIPTION OF THE DRAWINGS with the following replacement section:

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is an illustration showing a voltage-resistant distribution of a gate insulating film of a MISFET when no insulating film is formed on the back of a wafer.

FIG. 1B is an illustration showing a voltage-resistant distribution of a gate insulating film of the MISFET when an insulating film is formed on the back of the wafer.

FIG. 2 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing an example of a covering of an insulating film formed on the back of a wafer by using a single-wafer plasma-CVD system.

FIG. 3 is a graph showing the thickness of an insulating film covering the surface of a wafer from[[,]] an end portion of the surface of the wafer toward the central portion thereof.

FIG. 4 is an illustration of plan views and [[a]] partially cross-sectional views of the back of a wafer showing an insulating film formed on both the back and the bevel portion of the wafer.

FIG. 5 is a plan view of the back of a wafer showing an insulating film formed on the back of the wafer.

FIG. 6 is an illustration showing a voltage-resistant distribution of a gate insulating film of a MISFET when no insulating film is formed on the back and the bevel portion of a wafer.

FIG. 7A is an illustration showing a voltage-resistant distribution of a gate insulating film of a MISFET when an insulating film is formed on [[a]] both a partial area of the back and the whole area of the bevel portion of a wafer.

FIG. 7B is a plan view of the back of the wafer.

FIG. 7C is a cross-sectional view of the circumferential portion of the wafer.

FIG. 8A is an illustration showing a voltage-resistant distribution of a gate insulating film of a MISFET when a second insulating film is formed on the whole area of the back of a wafer.

FIG. 8B is a plan view of the back of the wafer.

FIG. 8C is a cross-sectional view of the circumferential portion of the wafer.

FIG. 9 is a schematic view for explaining a mechanism for reducing charge-up damages in a plasma treatment by forming an insulating film on the back of a wafer.

FIG. 10 is a schematic view for explaining a mechanism for reducing charge-up damages in a plasma treatment by forming an insulating film on the bevel portion of a wafer.

FIG. 11 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 12 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 13 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 14 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 15 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 16 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 17 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 18 is a cross-sectional view of ~~an essential~~ a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 19 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 20 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 21 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 22 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 23 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 24 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 25 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 26 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 1.

FIG. 27 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 2.

FIG. 28 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 2.

FIG. 29 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 2.

FIG. 30 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 2.

FIG. 31 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 3.

FIG. 32 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 3.

FIG. 33 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device which is embodiment 3.

FIG. 34 is a cross-sectional view of ~~an essential~~a principal portion of a substrate showing a manufacturing method of a CMOS device that is embodiment 3.

Page 18:

Please substitute the following paragraph for the paragraph beginning at line 18:

~~Then~~Next, a mechanism for reducing charge-up damages in a plasma treatment by forming an insulating film on the back of a wafer will be described below by referring to FIG. 9.

Page 19:

Please substitute the following paragraph for the paragraph beginning at line 4:

~~Then~~Next, a mechanism for reducing charge-up damages in a plasma treatment by forming an insulating film on the bevel portion of a wafer will be described below by referring to FIG. 10.

Page 19:

Please substitute the following paragraph for the paragraph beginning at line 8:

As shown in FIG. 10, when plasma becomes non-uniform on the main surface of the wafer 7, it is estimated that a potential difference occurs between plasma 8 ~~converting~~ covering the bevel portion of the wafer 7 and plasma 8a on the main surface of the wafer 7, and electric charges flow through bulk of the wafer 7, and thereby, for example, the

gate insulating film of a MISFET is broken (a second mode). Therefore, by forming an insulating film on the bevel portion of the wafer 7, it is possible to cut off a current path and suppress charge-up.

Page 20:

Please substitute the following paragraph for the paragraph beginning at line 13:

~~Then~~Next, a manufacturing method of a CMOS (Complementary Metal Oxide Semiconductor) device, which is the embodiment 1, will be described below according to the order of steps by referring to sectional views of ~~an essentiala~~ principal portion of a substrate shown in FIGs. 11 to 26.

Page 35:

Please substitute the following paragraph for the paragraph beginning at line 4:

(Embodiment 2)

A manufacturing method of a CMOS device that is ~~this~~ embodiment 2 will be described below by referring to cross-sectional views of ~~an essentiala~~ principal portion of a substrate shown in FIGs. 27 to 30 in step order. First, an n-channel MISFET and a p-channel MISFET are formed in accordance with the same manufacturing method as the case of

the above- mentioned embodiment 1, and then a silicon oxide film 21 is formed on the upper layers of the MISFETs. Then, an insulating film 22 is formed on the back of a substrate 11 and thereafter the surface of the silicon oxide film 21 is polished through, for example, a CMP method and the surface thereof is flattened. At the same time, particles are removed from the surface of the substrate 11. These steps are the same as those shown in FIGs. 11 to 17 for the embodiment 1.

Page 37:

Please substitute the following paragraph for the paragraph beginning at line 10:

(Embodiment 3)

A manufacturing method of a MOS device that is this embodiment 3 will be described below in step order by referring to cross-sectional views of ~~an essentiala~~ principal portion of a substrate shown in FIGs. 31 to 34. First, an n-channel MISFET and a p-channel MISFET are formed in accordance with the same manufacturing method as the case of the embodiment 1, and then a silicon oxide film 21 is formed over the upper layers of the MISFETs. These steps are the same as those shown in FIGs. 11 to 15 for the embodiment 1.